



A Low Noise and High Dynamic Range CMOS Integrated Electronics associated with Double Sided Silicon Strip Detectors for a Compton Camera gamma-ray Detecting System

M. Dahoumane, D. Dauvergne, J. Krimmer, J.-L. Ley, E. Testa, Y. Zoccarato

► To cite this version:

M. Dahoumane, D. Dauvergne, J. Krimmer, J.-L. Ley, E. Testa, et al.. A Low Noise and High Dynamic Range CMOS Integrated Electronics associated with Double Sided Silicon Strip Detectors for a Compton Camera gamma-ray Detecting System. NSS-MIC, Nov 2014, Seattle, United States. hal-01131450

HAL Id: hal-01131450

<https://hal.science/hal-01131450>

Submitted on 13 Mar 2015

HAL is a multi-disciplinary open access archive for the deposit and dissemination of scientific research documents, whether they are published or not. The documents may come from teaching and research institutions in France or abroad, or from public or private research centers.

L'archive ouverte pluridisciplinaire **HAL**, est destinée au dépôt et à la diffusion de documents scientifiques de niveau recherche, publiés ou non, émanant des établissements d'enseignement et de recherche français ou étrangers, des laboratoires publics ou privés.

A Low Noise and High Dynamic Range CMOS Integrated Electronics associated with Double Sided Silicon Strip Detectors for a Compton Camera gamma-ray Detecting System

Mokrane Dahoumane, D. Dauvergne, J. Krimmer, J.-L. Ley, E. Testa, Y. Zoccarato

Abstract— An 8-channel Front End integrated Electronics (FEE) circuit is designed and fabricated using the AMS-CMOS 0.35 μm process to equip a Compton camera system for quality control in Hadrontherapy. The circuit provides the energy deposited by prompt γ rays interacting in a 2 mm thick Double sided Silicon Strip Detector (DSSD), the (x,y,z) space coordinates and the time of the interaction. Each channel includes a Charge Sensitive Amplifier (CSA) followed by two parallel shapers. Slow and fast shapers, with 1 μs and 15 ns shaping time are used to measure the energy and time stamping, respectively. In order to increase the detection efficiency, a 3 bit multi-gain configuration is chosen to implement the fast shaper. The output of the latter is sent to a voltage comparator which provides a digital signal used as event time stamp and resetting signal of the CSA feedback capacitor to avoid pileup or circuit saturation. A 5 bit DAC is integrated to compensate any comparator offset dispersion between channels. A programmable digital circuit is also integrated in this design to adjust the delay and the width of the reset signal. All configuration settings are controlled by an I2C interface circuit which is integrated in the circuit. The present design provides the readout of the two sides of the DSSD thanks to a hole or electron configurable system. All the functionalities of the design have been successfully tested and validated. The test results are in good agreement with analytical and simulation calculations. A high linearity over a range of 3×10^3 to 3×10^6 electrons is reached with a conversion gain of 3.6 mV/fC. The circuit (CSA output) achieves an ENC (Equivalent Noise Charge) of 290 electrons rms. The circuit dissipates 23 mW/channel and occupies an area of $2 \times 4.5 \text{ mm}^2$, including pads.

I. INTRODUCTION

Several techniques to be used in hadrontherapy for cancer treatment worldwide are under study and development. The treatment consists in irradiating the tumorous cells with protons or ions. During irradiation, part of the incident projectiles undergoes nuclear fragmentation. Since excited fragments emit γ -rays almost instantaneously (below the ns range), the detection of prompt-gamma rays can be used to

monitor online the ion range [1], [2]. A Compton camera device has been proposed [3], [4], and is nowadays being one of the most attractive techniques thanks to its very high efficiency and fastness for the online dose control and high resolved 3D image reconstruction. In the proposed system shown in Fig. 1, the scatter detector is composed of a stack of 2×64 -strip Double sided Silicon Strip Detectors (DSSD) with a volume of $90 \times 90 \times 2 \text{ mm}^3$.

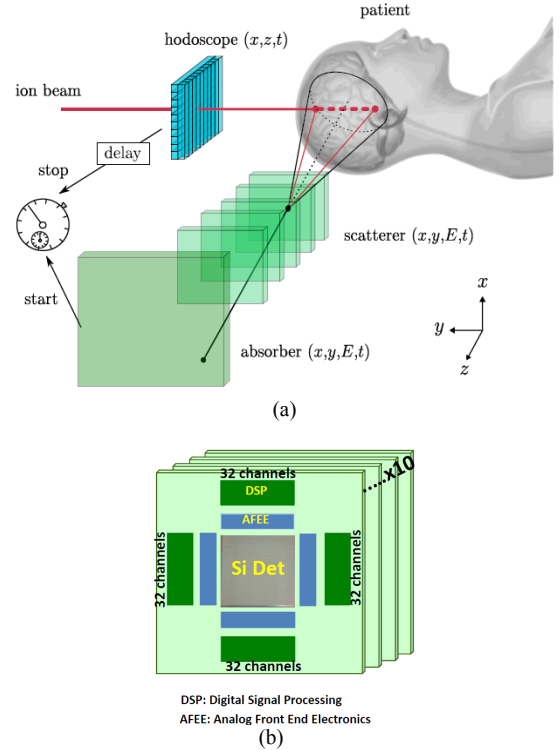


Fig. 1. Compton Camera device. (a): monitoring configuration system: the prompt γ -ray emission points are reconstructed by intersecting the ion trajectory, given by the hodoscope and the Compton cone, reconstructed with the Compton camera [4]. (b): zoom on the scatter detector composed of 10 planes of DSSD mounted on PCB EFF&DAQ card.

The detectors have been bonded and mounted on a PCB test board for characterization. First measurements of the leakage current as a function of temperature have already been done successfully. The scatter detector provides the spatial and temporal coordinates (x, y, z, t) and the energy deposited during the interaction of γ -rays. The DSSD detector will be

Manuscript received December 30, 2014.

This work is supported by the FP7-ENVISION program (grant agreement n°241851), the ANR Gamhadron project (ANR-09-BLAN-0106), the Rhône-Alpes Regional Program for Hadrontherapy Research, and the LabEx PRIMES (ANR-11-LABX-0063).

Mokrane Dahoumane, D. Dauvergne, J. Krimmer, J.-L. Ley, E. Testa, Y. Zoccarato are with the IPNL, Université de Lyon, F-69003 Lyon, France; Université Lyon 1 and CNRS/IN2P3, UMR 5822 F-69622 Villeurbanne, France. (corresponding author Tel.: +33 4 72 43 11 05. e-mail: m.dahoumane@ipnl.in2p3.fr)

- Low Equivalent Noise Charge (ENC) about 120 electrons rms (FWHM = 1 keV),
- Large dynamic range for both P&N polarities (from 3000 to 3000,000 electrons –N side),
- High occupancy rate: 10^5 hits/s per strip. This requires a fast switched system to avoid pile-up.

For this aim, a dedicated Front End Electronics (FEE) is designed and fabricated using the AMS CMOS 0.35 μm process. Hereafter will follow design details and test results of the realized circuit prototype.

II. DESIGN ARCHITECTURE

Fig. 2 shows a block diagram of a single channel of the circuit which is AC-coupled with a double sided DSSD detector. According to signal-to-noise ratio, and number of integrated functionalities, this circuit is an improved version and a complete system in comparison with the results of a previous version [5]. Each channel includes a Charge Sensitive Amplifier (CSA) followed by two parallel shapers. Slow and fast shapers, with 1 μ s and 15 ns shaping time are used to measure the energy and time stamping, respectively. In order to increase the detection efficiency, a 3 bit multi-gain configuration is chosen to implement the fast shaper. The output of the latter is sent to a voltage comparator which provides a digital signal used as event time stamp and resetting signal of the CSA feedback capacitor to avoid pileup or circuit saturation. During the reset phase, the outputs of the two shapers are fixed to a reference value. A 5 bit DAC is integrated to compensate any comparator offset dispersion between channels. A programmable digital circuit is also integrated in this design to adjust the delay and the width of the reset signal with 3 and 5 bit control signals, respectively. All configuration settings are controlled by an I2C interface circuit which is integrated in the circuit.

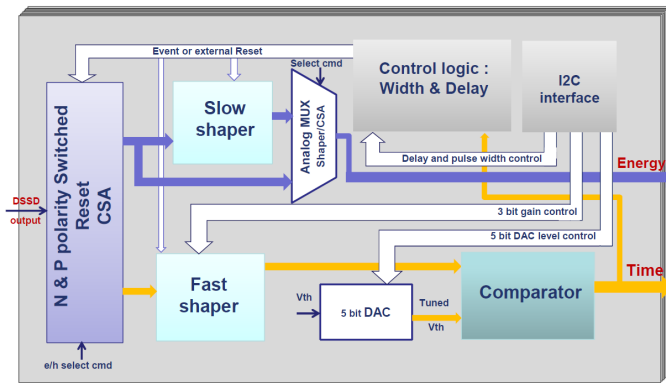


Fig. 2. Block diagram of a single channel of the readout electronics to be coupled with a double sided DSSD detector. The P and N strips are read with two different selectable configurations.

The present design provides the readout of the two sides of the DSSD thanks to a hole or electron configurable system. Indeed, a DC shift level diode was inserted between the source of the IN-NMOS transistor and the ground as shown in Fig. 3.

In order to determine the DSSD signal profile and thus the depth of interaction point in the silicon, the CSA output can be directly accessed.

The detector, with a capacitance C_d , produces charge pulses that are integrated on the CSA feedback capacitor C_f [5], [6], [7].

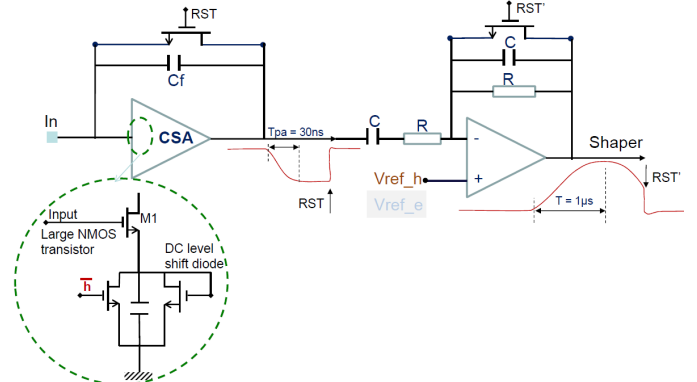


Fig. 3. CMOS switched reset feedback : illustration of a hole configuration by inserting a well dimensioned DC shift level Diode on the source of the input transistor of the CSA.

A. The Charge Sensitive Amplifier (CSA) description

Classical cascode architecture has been chosen to implement the CSA stage of the readout [5], [8]. The geometry of each component is optimized for the foreseen performances. The first order transfer function of the CSA in response to a pulse charge stimulus is given by:

$$\frac{V_{out}}{I_{in}}(\omega) = - \frac{Zf}{1 + j \frac{\omega C_d}{\omega_0 G_0 C_f}} \quad , \quad (1)$$

where, Z_f is the equivalent feedback impedance composed by R_{off} (very large) of the MOS switch in parallel with C_f . and C_d the detector capacitance. The value of C_f (250 fF) is fixed by the maximum signal of the dynamic range and the power supply voltage value which is 3.3 V in 0.35 μ m CMOS process we used.

An NMOS input transistor has been chosen to get a better power supply rejection ratio and higher speed than the PMOS one (more details were reported in the previous version of this design [5]). In order to minimize the ballistic deficit, $G_0 C_f$ has to be very superior to C_d ($G_0 C_f \gg C_d$), where G_0 is the open loop gain of the CSA, C_f the feedback capacitance and C_d the detector capacitance. To ensure up to 99 % of signal charge transfer, G_0 should be around 67 dB according to the following formula which gives the charge transfer rate α :

$$\alpha = \frac{1}{1 + \frac{C_d}{G_0 C_f}}. \quad (2)$$

The rise time of the CSA output for a pulse charge stimulus is determined by the amplifier time constant τ_{CSA} as:

$$\tau_{CSA} = \frac{C_d}{2\pi f_0 G_0 C_f} = C_d R_{in} \text{ ,} \quad (3)$$

where,

$$\omega_c = 2\pi f_0 G_0 \quad (4)$$

is the Gain Bandwidth Product.

A pole-zero R and C feed forward compensation technique is used to improve stability without affecting the speed of the CSA [9].

The authorized output dynamic range maintaining all transistors in the saturation mode is given by the approximate following formula:

$$V_{out} = \frac{-Q_{0max}}{C_f} = \frac{-480 fC}{250 fF} = -1.92 \text{ V}, \quad (5)$$

where Q_0 is the injected charge.

The total dynamic range corresponding to both polarities equals ± 1.92 V. So, a DC level shifting is needed in the case of P polarity (Cf. Fig. 3).

The CSA includes a source follower witch is needed to increase the driving capability.

B. The shaper implementation

A CR-RC signal shaping has been chosen to implement the two shapers (Cf. Fig. 3). Active shaping is performed by using a two stage compensated Miller OTA (Operational Transconductance Amplifier) [5]. The shaping stages perform a pulse shaping primarily to optimize the signal-to-noise ratio (SNR) of the system and also to measure the energy and the time with the slow shaper around 1 μ s shaping time and the fast one with a shaping time of 15 ns, respectively.

CR-RC shaper transfer function in the frequency domain is given by:

$$H(s) = \frac{\tau s}{(1 + \tau s)^2}, \quad (6)$$

where, τ is the shaping time. Here, we chose the derivation and the integration time constants to be equal (Cf. Fig. 3):

$$\tau_{shaping} = C \times R. \quad (7)$$

III. NOISE STUDY

A. Noise calculation

The most critical issue in this design is the noise. The desired energy resolution of the Compton camera which gives an acceptable spatial resolution of the whole hadrontherapy system must be below 1 keV FWHM. This corresponds to an input ENC (Equivalent Noise Charge) of 120 electrons rms.

Generally, there are two main sources of noise in a CSA: a parallel and a series noise. The parallel noise is generated by the thermal noise of the feedback resistor and the detector leakage current fluctuations. The input referred power spectral density (PSD) of the parallel noise is given by:

$$S_i(\omega) = 2qI_G + \frac{4kT}{R_f} = i_n^2, \quad (8)$$

where, q is the electron elementary charge, I_G is the detector leakage current, k is the Boltzmann constant and T is the temperature.

In this design, the feedback resistor was removed and replaced by a MOS switch. Therefore, this source of noise which represented 75% of the total noise in the previous design related in [5] has been canceled.

The noise input voltage spectrum (series noise PSD) of a MOS transistor in saturation is given by:

$$S_v(\omega) = \frac{8kT}{3g_m} + \frac{K_f}{C_{ox}WLf} = e_n^2 + \frac{A}{f}. \quad (9)$$

The first term is the channel thermal noise and the second term is the 1/f or Flicker noise [10]. Optimal noise matching is found by varying input transistor dimensions.

Total (series and parallel) noise output voltage spectrum is given by:

$$S_{out}(\omega) = \left(1 + \frac{C_d}{C_f}\right)^2 \left(e_n^2 + \frac{A}{f}\right) + \frac{i_n^2}{\omega^2 C_f^2}. \quad (10)$$

This formula is obtained through the following approximations: infinite open loop gain of CSA and considering an ideal integrator (i.e. no feedback resistance).

The output noise voltage of the complete chain is performed by integrating the product of CSA's output PSD by the shaper's Transfer function as in:

$$V_{out}^2 = \int_0^\infty S_{out}(\omega) |H(j\omega)|^2 \frac{d\omega}{2\pi}. \quad (11)$$

Total input referred noise after shaping is given by:

$$ENC = e_n \frac{C_t}{\sqrt{\tau}} \frac{e}{\sqrt{8}} \oplus in \sqrt{\tau} \frac{e}{\sqrt{8}} \oplus \sqrt{\frac{K_f}{C_{ox}WL}} C_t \frac{e}{2\sqrt{\pi}}, \quad (12)$$

where, C_t is the total input capacitance composed mainly by C_d and grid-source C_{gs} capacitance of the CSA input transistor, τ is the filtering time constant (shaping time).

In this design, calculations were done to find the optimal value of W/L of the input transistor leading to the best trade-off between minimizing series and 1/f noise and maintaining low value of C_t .

B. Noise simulations

To simulate the noise of a switched system, a transient noise simulation method is recommended, the drawback of this method is its high simulation time.

Fig. 4 shows the transient noise response of the CSA to the same injected charge using Cadence tool: 75 sweeps are used. The CSA was configured in the electron functioning mode.

There is different ways to calculate the noise on the Fig. 4. Best noise results are obtained by combining a CDS (Correlated Double Sampling) and averaging techniques. First an interval on the curve is selected and an average of the values is calculated by choosing number of samples. Then, the signal amplitude is the difference between the hit signal and its base line (Cf. Fig. 4). The standard deviation σ of the amplitudes is then calculated. The noise is given by:

$$ENC = \frac{\sigma}{(gain \times q)}, \quad (13)$$

where, gain is the CSA conversion gain given in mV/fC and q is the elementary charge. More statistics increase obviously the result, but at the expense of the counting rate. So, a compromise is to be found between counting rate and noise. This method gave an ENC noise of 105 electrons (rms), with CSA conversion gain = 3.5 mV/fC and $\sigma = 59.2 \mu\text{V}$.

The same method has been used to measure the noise (electrically) in the test.

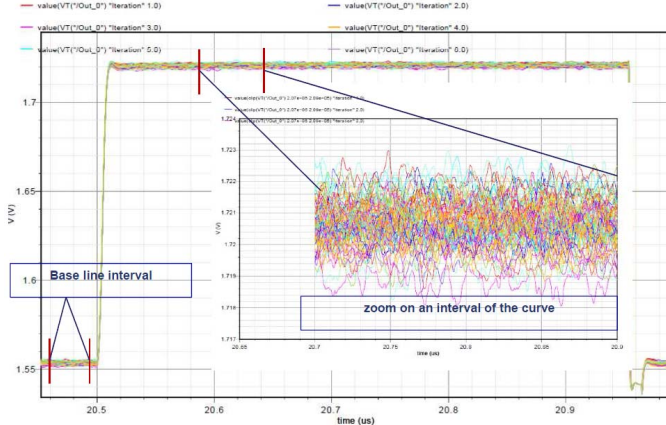


Fig. 4. Transient noise response of the CSA (75 simulation iterations), configured in electron functioning mode.

IV. LAYOUT DESIGN

The multi-channel nature of the design which will fit the form of the strips of the DSSD detector (crosstalk issue), low noise and high speed are parameters that require a special care when drawing the layout of the input stage (CSA). Therefore, the R_{in} must be minimized by splitting the input transistor into a matrix of small transistors perfectly identical. The size of each channel has exactly the width of a pad (100 μm). This makes the channel multiplication easier and minimizes the mismatch between channels.

Fig. 5 shows the layout of the ASIC, an emphasis of the input transistor of the CSA is carried out.

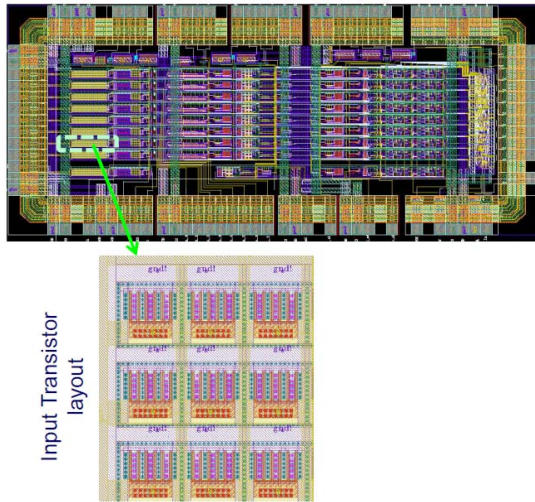


Fig. 5. Layout of the full chip fabricated in CMOS 0.35 μm process of AMS: a zoom on the CSAs' input transistor is shown.

V. EXPERIMENTAL RESULTS

A prototype has been fabricated in a CMOS 0.35 μm process from Austria Micro System. It includes 8 channels of the described FEE readout of the Compton camera. A photography of the chip is shown in Fig. 6.

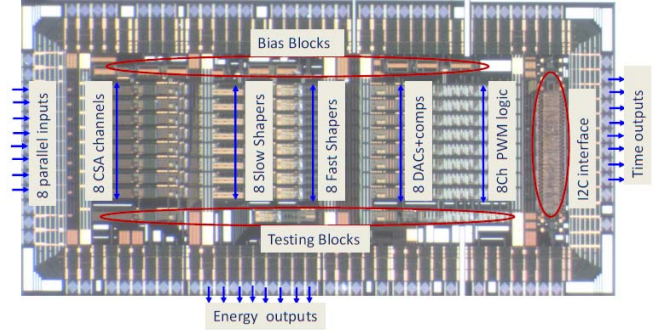


Fig. 6. Photography of the chip showing its various blocks: 8 parallel complete channels, bias blocks and individual testing blocks.

The circuit dissipates a power of 23 mW per channel from 3.3 V supply voltage and occupies an area of $2 \times 4.5 \text{ mm}^2$, including pads.

A. Test setup

A test board was designed to characterize the prototype experimentally. Fig. 7 shows a photography of the test board and a synoptic of its modules. A charge injection circuit is used to simulate the detector charge which will be generated by the stopping of a Compton recoil electron in the DSSD.

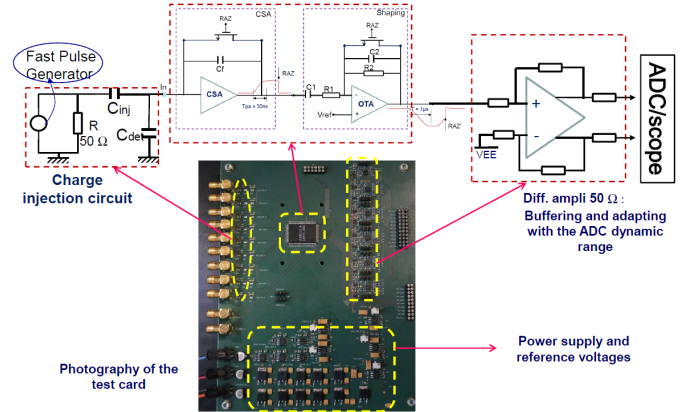


Fig. 7. Test set up and photo of the test board supporting the ASIC (device under test). On the top, is shown a synoptic of the test board.

This circuit is composed of a fast pulse generator terminated by a 50 Ω resistor, a 1 pF injection capacitor and a 10 pF capacitor to simulate the detector capacitance. The response of the ASIC to an input pulse is sent to a 50 Ω fully differential buffering stage to drive different signal processing devices (e.g. scope, external amplifiers, ADCs...).

B. Test results and circuit performances

The circuit has been successfully tested. The test results are in good agreement with analytic and simulation calculations. All the functionalities have been validated.

Fig. 8 shows output waveforms of the circuit for both negative and positive signal polarities. The measured shaping time of the slow shaper is $0.9 \mu\text{s}$. The measured rise time of the CSA is 30 ns in response to a fast pulse injected charge. The CSA is fast enough to follow the incoming charge signal without modifying its shape.

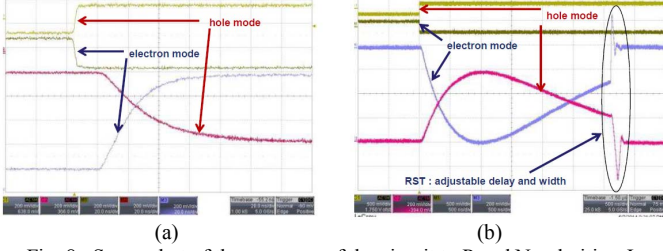


Fig. 8. Screenshot of the response of the circuit to P and N polarities. In (a) is shown the CSA output and in (b) the CSA+slow shaper output.

Linearity measurement was also performed and shown in Fig. 9. The top of the figure shows the measured and simulated CSA outputs as a function of the input charge (in fC). The bottom of this figure shows the measured and simulated output of the chain including CSA and slow shaper. On the left side is shown the electron mode and on the right the hole mode functioning of the circuit.

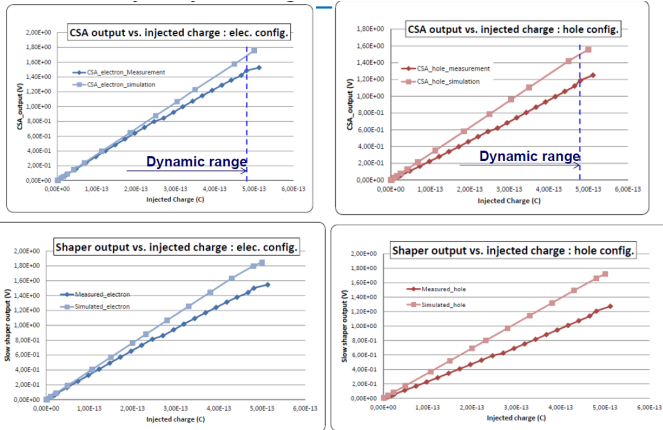


Fig. 9. Output vs. injected charge (Q_{inj}) response of the CSA for N and P polarities on the top side. Output vs Q_{inj} response of a complete chain (CSA followed by slow shaper) for N and P polarities on the bottom of the figure.

The circuit achieves a high linearity even over the needed dynamic range, mostly less than 1 % of INL with a conversion gain of 3.6 mV/fC , which is very close to the simulation one. The noise evaluation has been performed according to the measurement standards. Noise and signal were measured in the same conditions (temperature and electromagnetic environment).

An ENC of 290 electrons rms was measured for electron configuration on the output of the CSA. The ENC measured on the slow shaper output is about 390 electrons rms (electron configuration). The performances obtained for the hole configuration are slightly lower than those achieved for the

electron one. This is due to the DC shift level diode used in case of P polarity (Cf. Fig. 3).

The parallel disposition and neighborhood of channels gives a cross talk of 0.6 %, mostly (>90%) coming from the supply voltage disturbance.

C. Time measurements and digital part testing

The time measurement is performed on the fast shaper's branch of a readout channel. As said above, the fast shaper is followed by a fast comparator. The latter provides a digital signal used for time stamping and reset signal. A digital part is integrated in the chip to control the width of the reset signal and its occurrence delay. In order to bypass the comparator offset dispersion problems, a 5bit DAC has been integrated. It tunes the reference voltage of the comparator of each channel individually. All these parameters are controllable thanks to I2C interface witch is integrated in this prototype.

The tests of all these modules have been successfully performed. Among them: comparator S-curves, DAC linearity, I2C writing and reading frames, fast shaper gain. The digital part is thoroughly tested, because it is very important to control the instant of the reset separately for the CSA and the shaper. The width of the shaper reset must be larger than the CSA one. This was verified and validated in the tests.

D. Detector readout system

After electrical characterization, the ASIC was coupled to a 64-strip double-sided SSD detector to measure the energy spectrum of radioactive sources (e.g. ^{133}Ba providing photon lines at 30.9, 53, 80.9, 276, 303, 356 and 383 keV). Fig. 10 shows a photography of the PCB card designed to support mechanically and to bias the detector. This mezzanine card will be mounted on a data acquisition (DAQ) mother card in the way shown in Fig.1-b. The DAQ card is being manufactured.

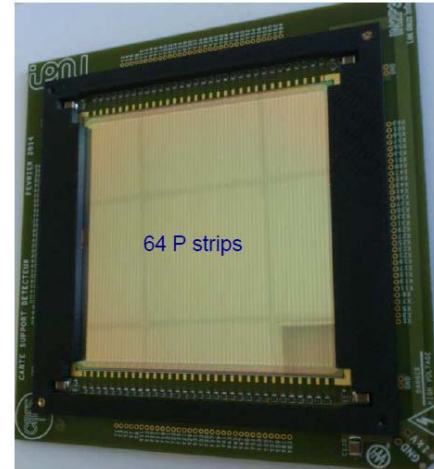


Fig. 10. Photography of the silicon detector bonded on a PCB mezzanine card. The P and N strip are ac-coupled with the readout ASICs. Bias resistors are also mounted on this card.

TABLE I gives a summary of the circuit performances. The measured parameters are close to schematic simulation ones. The values of the measured noise include the setup and the

scope noise. This explains the difference between simulations and measurements in terms of noise.

TABLE I. PERFORMANCE SUMMARY

		Sch. Simu.	Test
Power supply	Both polarities	3.3 V	3.3 V
CSA input transistor current (85% of the total consumption)	Both polarities	5 mA	5 mA
CSA conversion gain (mean)	electrons	3.63 mV/FC	3.25 mV/FC
	holes	2.83 mV/FC	2.25 mV/FC
CSA Noise (ENC) rms	electrons	105 e- rms (transient noise simulation)	290 e- rms
	holes	435 e- rms (transient noise simulation)	560 e- rms
CSA-Slow Shaper conversion gain	electrons	4.35 mV/FC	3.6 mV/FC
	holes	3.85 mV/FC	3 mV/FC
CSA-Slow Shaper Noise (ENC) rms	electrons	-----	390 e- rms
	holes	-----	630 e- rms
Shaping Time (slow shaper)	electrons	0.9 us	0.9 us

VI. CONCLUSION AND OUTLOOK

An 8-channel front end readout electronics has been designed and fabricated in 0.35 μm CMOS process from AMS. It will readout the signals delivered by the Silicon Strip Detectors constituting the Compton camera for prompt-gamma monitoring of hadrontherapy. The test of this prototype has given very satisfactory results and has validated all the functionalities and features of the circuit. By using a switch-reset technique, parallel noise that could be generated by a feedback resistance is removed. In contrast, the complexity of the design is increased. Noise measurement setup is being optimized in order to get better results. In the final design of a plane composing the scatter detector the analog signal of the ASIC will be directly sent to an ADC. So, the scope and the setup noise will be canceled. Production of 180 additional chips is scheduled for February 2015, to equip all the scatter detectors.

REFERENCES

- [1] C.-H. Min, C. H. Kim, M.-Y. Youn, et J.-W. Kim, « Prompt gamma measurements for locating the dose falloff region in the proton therapy », *Appl. Phys. Lett.*, vol. 89, no. 18, p. 183517-3, oct. 2006.
- [2] E. Testa, M. Bajard, M. Chevallier, D. Dauvergne, F. Le Foulher, N. Freud, J.-M. Létang, J.-C. Poizat, C. Ray, et M. Testa, « Monitoring the Bragg peak location of 73 MeV/u carbon ions by means of prompt γ -ray measurements », *Appl. Phys. Lett.*, vol. 93, no. 9, p. 093506, 2008.
- [3] M.-H. Richard, M. Chevallier, D. Dauvergne, N. Freud, P. Henriquet, F. Le Foulher, J. M. Létang, G. Montarou, C. Ray, F. Roellinghoff, E. Testa, M. Testa, et A. H. Walenta, « Design Guidelines for a Double Scattering Compton Camera for Prompt-gamma imaging During Ion Beam Therapy: A Monte Carlo Simulation Study », *IEEE Transactions on Nuclear Science*, vol. 58, no. 1, p. 87-94, févr. 2011.
- [4] F. Roellinghoff, M.-H. Richard, M. Chevallier, J. Constanzo, D. Dauvergne, N. Freud, P. Henriquet, F. Le Foulher, J. M. Létang, G. Montarou, C. Ray, E. Testa, M. Testa, et A. H. Walenta, « Design of a Compton camera for 3D prompt-gamma imaging during ion beam therapy », *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, vol. 648, no. Supplement 1, p. S20-S23, août 2011.
- [5] M. Dahoumane, D. Dauvergne, J. Krimmer, H. Mathez, C. Ray, E. Testa, A.H. Walenta, Y. Zoccarato, « A Low Noise and High Dynamic Charge Sensitive Amplifier-Shaper associated with Silicon Strip

- Detector for Compton Camera in hadrontherapy”, 2012 Nuclear Science Symposium, Medical Imaging Conference Record (NSS/MIC).
- [6] Paul O'Connor and Gianluigi De Geronimo, “Prospects for charge sensitive amplifiers in scaled CMOS”, *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, Volume 480, Issues 2–3, 21 March 2002, Pages 713–725.
- [7] R. Hofmann and G. Lutz, “Development of readout electronics for monolithic integration with diode strip detectors”, *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, Volume 226, Issue 1, 15 September 1984, Pages 196–199.
- [8] V. Radeka, P. Rehak et al., “Design of a charge sensitive preamplifier on high resistivity silicon,” *IEEE Trans. Nuclear Science*, vol.35, no.1, pp.155-159, Feb. 1988
- [9] W. Sansen and Z. Y. Chang, “Feedforward Compensation techniques for High Frequency CMOS amplifier”, *IEEE J. Solid-State Circ.*, vol. 25, N°6, pp.1590-1595, December 1990.
- [10] W.M.C Sansen and Z.Y. Chang, “Limits of low noise performance of detector readout front ends in CMOS technology”, *IEEE Transactions on Circuits and Systems*, Volume: 37 , Issue: 11 Nov 1990 Page(s): 1375 – 1382.